REMARKS:

I. Status of the Application.

Following the above amendments, claims 1 – 5 and 7 – 143 are pending. Following an interview with the Examiner, the patent office agreed to withdraw the restriction requirement, and to examine the remaining claims (32 – 100) following this response. Claims 101 – 143 are new, and have been added to further clarify the new and novel integrated circuit architecture of the present invention.

In the September 6, 2005 Office Action (the "Office Action"), claims 1 – 33 were rejected, in various combinations, as: (1) directed to non-statutory subject matter under Section 101 (Office Action points 15 and 16); (2) anticipated under Section 102 based on Wise U.S. Patent No. 5,768,561 ("Wise" or the "Wise reference") (Office Action points 17 – 37); and (3) obvious under Section 103(a) over Wise in view of Lee et al. U.S. Patent No. 5,873,045 ("Lee" or the "Lee reference") (Office Action points 38 – 40).

In this response, Applicants have amended claims 1, 3, 4, 7 – 11, 14, 17 – 23, 25 – 32, 35, 41, 45, 63, 66, 71, 75, and 89 – 100, and have added new claims 101 – 143. Applicants respectfully traverse the rejection of claims 1 – 33 under Sections 101, 102 and 103(a). Applicants respectfully request reconsideration of the pending claims in view of the foregoing amendments and the following remarks.

II. The Rejection of Claims as Non-Statutory Should Be Withdrawn.

In the Office Action (points 15 and 16), claim 1 was rejected as directed to non-statutory subject matter. In light of the amendments adding a memory element for storage of configuration information, the claims are now limited to tangible embodiments, and the Section 101 rejection is not longer applicable and should be withdrawn.

III. The Rejection of Claims 1 – 33 Should Be Withdrawn.

In the Office Action, claims 1 – 33 were rejected, in various combinations, as anticipated under Section 102 or obvious under Section 103(a) based on the Wise reference or Wise in view of the Lee reference (Office Action points 17 – 40). For the reasons stated below, Applicants respectfully traverse the rejection of claims 1 – 33 under Sections 102 and 103(a), and request that the Examiner withdraw the rejection of these claims and further allow claims 1 – 5 and 7 – 143. As discussed in greater detail below, the cited references do not disclose all the limitations of the claimed invention and, in addition, teach away from the claimed invention.

A. The Claimed Invention.

The claimed invention provides a plurality of fixed and differing (*i.e.*, heterogeneous) computational elements that are configurable, through various levels of an interconnection network, to form a wide variety of functional or operational modes. The heterogeneous computational elements of the invention include fixed and differing IC architectures, such as fixed architectures for different functions such as memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability (see, *e.g.*, specification p. 3, ll. 5 – 9). The configuration of the plurality of heterogeneous computational elements is accomplished through an interconnection network, which selectively or differentially routes (via routing elements) data and configuration to the different groups of computational elements, and which changes the input and output connections (through switching elements) of the plurality of heterogeneous computational elements, connecting and reconnecting these computational elements in different configurations to perform different functions at different times (see, *e.g.*, specification, p. 13, ll. 10 – 20; p. 22, ll. 20 – 29). None of the cited references disclose or suggest an interconnection network having routing elements, and certainly none having both routing and switching elements.

The routing elements of the interconnection network are also utilized for configuration of the computational elements, by selectively or differentially routing data and configuration information to selected groups of computational elements (specification, p. 13, ll. 10 – 20). The interconnection network is also combined or

unitary network which can transmit both data and configuration information, as a stream or in packets, in contrast to prior art use of completely separate and independent data and configuration buses (specification, p. 13, ll. 10 – 20). The present invention also can utilize "self-routing" data and configuration, in which the routing elements themselves are adapted to select the appropriate route, rather than being under the control of a dedicated communication controller.

In addition, particular heterogeneous computational elements are preselected and grouped into computational units, and further differentially grouped into matrices, for configurable performance of a corresponding plurality of different functions (see, *e.g.*, specification p. 21, ll. 1 – 29). For example, one set of heterogeneous computational elements may be selected and configured to form a matrix for performance of an FFT, while a second and different set of heterogeneous computational elements may be selected and configured to form a matrix for bit manipulation, such as Viterbi decoding. The resulting reconfigurable matrices, using different mixes and layouts of these fixed and different computational elements, therefore have different architectures. This is in stark contrast to the prior art of reconfigurable or field programmable devices, which utilize arrays of identical, repeating sub-units or arrays of the same exact architecture of reconfigurable elements.

The claimed invention also utilizes "nested" levels of configuration and reconfiguration of these heterogeneous computational elements, through multiple levels of interconnection networks. For example, a first matrix of heterogeneous computational elements having a first functionality is formed through a first interconnection network, and a second matrix of heterogeneous computational elements having a second functionality is formed through a second interconnection network. In turn, a third interconnection network is capable of configuring and reconfiguring these first and second matrices for a plurality of functional or operating modes, creating this multi-tiered or "nested" reconfigurability (see, *e.g.*, specification p. 14, ll. 3 – 19).

B. Novel and Non-Obvious Features of the Claimed Invention.

There are several new and non-obvious features of the invention as claimed, which are not disclosed in any of the cited references, for this patent application

and for related patent applications, based upon the searches performed by the patent offices of both the U.S. and Europe. As discussed in greater detail below, none of the prior art references disclose or suggest, in any way, the following novel and non-obvious features of the present invention:

(1) the interconnection network comprises both routing elements and switching elements, in contrast to prior art use of switching elements only;

(2) the routing elements of the interconnection network are also utilized for configuration, in contrast to prior art use of switching elements only (and which does not disclose or suggest any form of such routing);

(3) the interconnection network is a combined network which can transmit both data and configuration information, in contrast to prior art use of completely separate and independent data and configuration buses;

(4) the interconnection network can transmit both data and configuration information as packets, and can utilize data commingled with configuration information as a single bit stream or as a combined packet structure (in contrast to prior art, which does not disclose or suggest such packet transmission);

(5) the present invention utilizes different mixes or combinations of different computational elements forming independently configurable groups, in contrast to prior art use of a repeating array of the same group of computational elements;

(6) "nested" or multiple levels of configuration are utilized, in contrast to the prior art (which does not disclose or suggest such multiple levels of configuration); and

(7) the present invention can utilize "self-routing" data and configuration, in which the routing elements themselves are adapted to select the appropriate route, rather than being under the control of a dedicated communication controller.

The independent claims 1, 32, 63, 89, 91, 93, and 94, as amended, and new independent claims 129 and 139, claim these new and novel features. Support for the various amendments may be found throughout the specification and Figures, and are cited above in the previous section. These new and non-obvious features have been claimed, in various combinations, as follows:

(A) Independent system claim 1 has been amended to claim that the interconnection network comprises both routing elements and switching elements, and that the interconnection network can separately configure at least two different groups of computational elements for different functions (novel features 1 and 5, above).

(B) Independent method claims 32 and 63 have been amended to claim that the interconnection network provides selective routing of both data and configuration information and that the interconnection network can separately configure at least two different groups of computational elements for different functions (novel features 3 and 5, above).

(C) Independent apparatus claim 89 has been amended to claim that the interconnection network is a combined network which can transmit both data and configuration information (novel feature 3, above).

(D) Independent apparatus claim 91 has been amended to claim that the interconnection network comprises both routing elements and switching elements, that the interconnection network is a combined network which can transmit both data and configuration information, and that the interconnection network can separately configure at least two different groups of computational elements for different functions (novel features 1, 3 and 5, above).

(E) Independent apparatus claim 93 has been amended to claim that the interconnection network comprises both routing elements and switching elements, that both the routing elements and switching elements of the interconnection network are also utilized for configuration (novel features 1 and 2, above).

(F) Independent apparatus claim 94 has been amended to claim that the interconnection network comprises a plurality of routing elements and configures the computational elements (novel feature 1, above).

(G) New independent claim 129 has been added to claim that the interconnection network is a combined network which can transmit both data and configuration information (novel feature 3, above), with new dependent claims to claim the various remaining novel features 2 through 8.

(H) Independent system claim 139 has been added to claim that the interconnection network comprises both routing elements and switching elements, and that the interconnection network can separately and independently configure at least two different groups of computational elements for different functions by the selective routing or switching of data (novel features 1, 2 and 5, above), with new dependent claims to claim the various remaining novel features 2 through 8.

(I) Additional dependent claims have been added to claim the remaining novel features 2 through 8, with new claims 101 – 114 depending from independent claim 94, new claims 115 – 128 depending from independent claim 1.

As discussed in greater detail below, the heterogeneous computational elements having fixed and differing architectures, which are configurable through both routing elements and switching elements of an interconnection network, for multiple and different functions, as claimed, are not present in the prior art. The prior art also does not disclose utilizing an interconnection network for transfer of both data and configuration information; rather, all of the prior art references utilize separate, dedicated and independent data and configuration buses. In addition, the prior art does not disclose using different mixes and layouts of these fixed and different computational elements, to form larger reconfigurable matrices, which are also heterogeneous. The prior art does not disclose or suggest the multi-tiered or "nested" reconfigurability of these heterogeneous computational elements through the interconnection network. Rather, the cited prior art merely discloses programmable arrays of identical computational units each having precisely the same internal architecture.

C. The Cited Prior Art Does Not Disclose or Suggest the Claimed Features of the Invention.

The Wise reference does not disclose or suggest any of these claimed features of the invention. First, Wise does not disclose use of an interconnection network which transfers both data and configuration information; rather, for all embodiments, Wise utilizes separate data and control lines (see, *e.g.*, Figure 27, control line 327, data line 328, Figure 118, Col. 13, Col. 21 - 22), and further specifically utilizes a dedicated, 2-wire interface and an "extension bit" line for control. Second, Wise does not utilize

any type of interconnection network – Wise does not utilize any routing elements and does not utilize any switching elements for configuration or reconfiguration. For example, the reconfigurable processing stage illustrated in Wise Figure 10 has no interconnection network, routing or other switching elements, only fixed data path 35 and control lines 37. See also Wise Figure 27 (fixed data line 328 and fixed control line 327) and Figure 118. The most Wise discloses is the forking or branching of an output to multiple inputs but, again, none of these data path connections are multiplexed or otherwise switched or routed.

This is not surprising, because the invention of the Wise reference involves a very different type of configurability than that of the present invention. Simply, the Wise reference does not provide for switchable or routable data paths for configuration. Rather, the reconfiguration of Wise is provided in two ways for reconfiguration for different standards (such as MPEG or JPEG): first, different values are loaded into a look-up table, which are then fetched to provide the reconfiguration (Figure 15, Figure 80 (JPEG and MPEG tables), Col. 44 – 45 identical state machine circuitry is utilized, with different memory addresses to tables for each standard); and second, different start addresses are provided for microcode to be executed by the various instruction processing ALUs (*e.g.*, 32-bit microcode instruction processor Huffman ALU of Figure 126 and Col. 229-230). In all of these instances, a fixed data path and fixed logic are utilized, with dedicated processing blocks controlled by a programmable state machine (Col. 200). In addition, the "addressing" of Wise is not for routing; rather, such "addressing" indicates data type (Col. 27). Multiplexing is only utilized in Wise to select which values are utilized for comparison, not for routing of data paths (Col. 221 - 222). In fact, Wise specifically excludes any complex switching or multiplexing for the IDCT architecture (Col. 262, ll. 34-35 and Fig. 137) and, as a consequence, specifically *teaches away* from the present invention. As a consequence, a Huffman decoder in Wise is always a Huffman decoder, just with different input values from table look-ups and different instructions for implementing different standards, and never reconfigures data input and output paths to becomes another type of decoder such as a Viterbi decoder.

Figure 137 of Wise was specifically cited for illustration of configurability. As illustrated in Figure 137, all of the input and output data paths are

fixed, and all of the functionality is fixed and non-configurable: for example, the carry-save adder/subtractor is always a carry-save adder/substractor, is never reconfigured to have any other functionality, and is never reconfigured with other elements to create other, combined functionality. The X and Y notations are not different functional modes, just the input and output for the duplication of the fixed combinational logic for the top and bottom halves of Figure 136 (Col. 262, ll. 14-19). The "common block" is dedicated, fixed combinational logic, and is not an interconnection network of any kind. Similarly, none of the interconnections among these computational elements is ever changed to create different functionality. Rather, Figure 137 is always the IDCT architecture, and is never reconfigured, for example, to perform an FFT, even though similar butterfly logic could be utilized.

More importantly, nothing in Wise discloses or suggests the claimed features of the present invention discussed above. Wise does not disclose or suggest, for example, any of the following claimed features: (1) an interconnection network comprising both routing elements and switching elements; (2) using routing elements for configuration; (3) using an interconnection network for transfer of both data and configuration information; (4) using an interconnection network for data commingled with configuration information as a single bit stream or as a combined packet structure; (5) different mixes or combinations of different computational elements forming independently configurable groups; (6) "nested" or multiple levels of configuration; and (7) "self-routing" of data and configuration. In the interest of brevity, the remaining claimed features which are also not disclosed or suggested in the Wise reference will not be discussed further.

The Lee reference pertains to use of cellular telephone for additional purposes, such as a portable communication interface (wireless transceiver) for a computer, using an intermediate structure referred to as a "holster", using the existing command structure of the particular cell phone. The mobile device of Lee does not perform multiple mobile client functions such as paging, PDA or multimedia reception; these functions are cited in Lee as examples of mobile clients only (Col. 3, ll. 2-16), with the mobile client of Lee being limited to a cell phone or other radio transceiver. Lee does not disclose any type of configurable or reconfigurable architecture. The Lee reference

does not disclose any type of configuration information (at cited Col. 8, ll. 46-51 or elsewhere) which would provide for the switching or routing of input and output data paths, and certainly does not disclose the commingling of such configuration information with data to form a singular bit stream or data packet. Lee further does not disclose any of the claimed features (1) through (7) listed above. The Lee reference, therefore, is not relevant to adaptive, configurable or reconfigurable computing architectures and, more particularly, is not pertinent to the claimed present invention.

The remaining reference cited reference, Widergren et al. U.S. Patent No. 4,302,775 ("Widergren") (Office Action point 41) is also not relevant to the claimed invention. Widergren pertains to adaptive rate coding of data, and does not pertain to reconfigurable computing IC architectures.

As a consequence, the Wise reference, alone or in combination with the Lee or Widergren references, does not anticipate and does not render obvious the claimed invention. The claimed invention, therefore, is allowable over the Wise, Lee, Widergren, and other references discussed below.

D. The Cited Prior Art of Related Applications Also Does Not Disclose or Suggest the Claimed Elements of the Invention.

Additional references have been cited in the examination of related patent applications before the United States Patent and Trademark Office, the PCT, and the European Patent Office, which also do not disclose and do not suggest all of the limitations of the claims of the present invention. The references are listed on the supplemental information disclosure statement, with copies of all publications (other than US patents) provided, and are discussed below.

The PCT Search Report of a related, commonly assigned application, U.S. Patent Application Serial No. 09/997,987, filed November 30, 2001 (the "first related application), and its corresponding PCT/US02/37013, disclosed Kopp et al. U.S. Patent No. 5,450,557 ("Kopp" or the "Kopp reference"). The Kopp reference utilizes different processing elements connected to input and output registers, with multiplexers changing connections between the various registers, programmed through a very long word instruction. Kopp does not disclose or suggest all of the limitations of the independent

claims of the present invention, such as the configuration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions. Kopp utilizes separate data and configuration buses, using a data bus and separate, dedicated selection lines to multiplexers. Kopp does not disclose the interconnection network of the present invention, as discussed below. Kopp also does not disclose or suggest using different mixes and layouts of these fixed and different computational elements to form differing reconfigurable matrices for different functional and operational modes, or the multi-tiered or "nested" reconfigurability of these heterogeneous computational elements.

More specifically, Kopp does not disclose or suggest any of the following claimed features of the present invention: (1) an interconnection network comprising both routing elements and switching elements; (2) using routing elements for configuration; (3) using an interconnection network for transfer of both data and configuration information; (4) using an interconnection network for data commingled with configuration information as a single bit stream or as a combined packet structure; (5) different mixes or combinations of different computational elements forming independently configurable groups; (6) "nested" or multiple levels of configuration; and (7) "self-routing" of data and configuration.

Hui Zhang et al., "A 1V Heterogeneous Reconfigurable Processor IC for Baseband Wireless Applications (2000 IEEE International Solid-State Circuits Conference) (the "Zhang reference") was cited in the EPO examination for the cross-referenced related U. S. Patent Application Serial No. 09/815,122, filed March 22, 2001, now U.S. Patent No. 6,836,839 (the "second related application). The Zhang reference discloses a reconfigurable IC having satellite processors of different granularities (*e.g.*, MAC, ALU) connected by a reconfigurable interconnect. The interconnect is a 2-level hierarchical, mesh-structure having switchboxes (FPGA-type pass-transistors) which is configured through a separate 32-bit configuration bus (Fig. 4.1.1). The Zhang reference also does not disclose and does not suggest the claimed features (1) – (7) above. More particularly, the Zhang reference does not disclose or suggest a singular interconnect network for transfer of both data and configuration, an interconnect network having both

routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, etc.

Ahmad Alsolaim et al., "Architecture and Application of a Dynamically Reconfigurable Hardware Array for Future Mobile Communication Systems" (Field-Programmable Custom Computing Machines, 2000 IEEE Symposium on Napa Valley, CA, USA, 17-19 April 2000, IEEE Comput. Soc., US, 17 April 2000, pp. 205-214) (the "Alsolaim reference) was cited in a supplemental, September 2005 EPO search report for the first related application. The Alsolaim reference discloses an array of identical reconfigurable processing units (RPUs) connected to a hierarchical, switching interconnect (SRAM-based switching box, Figure 6). Different functions can be mapped to the individual components of the identical RPUs (Figure 9 and p. 212). The switching interconnect is controlled through a dedicated configuration bus from a global communication unit (GCU) to communication switching units (CSU), which in turn control the configuration memory units (CMUs) which provide configurations to the switching boxes (Figure 2 and p. 208). Separate and dedicated data input and output lines are coupled to the interconnect lines, in addition to direct connection to nearest neighbors. Having a switching data interconnect completely separate from a configuration bus, the Alsolaim reference teaches away from the present invention.

The Alsolaim reference also does not disclose and does not suggest the claimed features (1) – (7) above. More particularly, the Alsolaim reference does not disclose or suggest a singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, etc. In addition, the Alsolaim reference does not disclose the use of different mixes or combinations of computational elements to form different reconfigurable matrices, and instead utilizes a repeating array of identical structures.

Mohan et al. U.S. Patent No. 6,047,115 ("Mohan" or the "Mohan reference") was also cited by the EPO for the first related application. Mohan discloses an FPGA which utilizes two types of instructions, computational and pattern manipulation. Computational instructions provide for computing with data in pre-defined

memory locations. Pattern manipulation instructions move data into different memory locations to create a pattern for the next instruction. The Mohan reference is inapplicable to the claimed invention, and also does not disclose and does not suggest the claimed features (1) – (7) above, such as the singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, etc.

Jergen Becker et al., "Design and Implementation of a Coarse-Grained Dynamically Reconfigurable Hardware Architecture" (VLSI 2001, Proceedings. IEEE Computer Society Workshop on April 19-20, 2001, 19 April 2001 pp. 41-46) (the "Becker" reference) was also cited by the EPO for the first related application. The Becker reference discloses additional IC development from one or the co-authors of the Alsolaim reference, was published after the claimed priority date of the present invention, and is not available as prior art herein. Nonetheless, the Becker reference does not disclose any additional information relevant to the present invention, beyond that already discussed for the Alsolaim reference. More particularly, the Becker reference discloses the identical reconfigurable architecture of the Alsolaim reference, with additional application to Rake receivers. The Becker reference also makes more explicit the separate, direct connections from the configuration memory to the reconfigurable processing units, (Figure 3, p. 43), separate from the switchable data paths, which teaches away from and does not disclose the interconnect network structure of the present invention. Consequently, the Becker reference also does not disclose and does not suggest the claimed features (1) – (7) above.

V. Baumgarte et al., "PACT XPP – A Self-Reconfigurable Data Processing Architecture" 25 June 2001, XP-002256066 (retrieved online at http://www.pactcorp.com/xneu/download/ersa01.pdf) (the "Baumgarte reference") was cited in a supplemental EPO search report for the present invention, but was published after the claimed priority date of the present invention, and is not available as prior art herein. Nonetheless, the Baumgarte reference does not disclose or suggest the claimed features of the present invention. More particularly, the Baumgarte reference discloses an array of identical "processing array clusters" (PACs) having coarse-grained computing

elements, with a packet-oriented data network, a separate configuration bus, and distributed, hierarchical tree of configuration managers (see Figure 1. The packets are either data or event information (state information to control ALU execution).

The Baumgarte reference also does not disclose and does not suggest the claimed features (1) – (7) above. More particularly, the Baumgarte reference does not disclose or suggest a singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, etc. In addition, the Baumgarte reference does not disclose the use of different mixes or combinations of computational elements to form different reconfigurable matrices, and instead utilizes a repeating array of identical reconfigurable circuits.

Arthur Abnous et al., "Ultra-Low-Power Domain-Specific Multimedia Processors" (VLSI Signal Processing, IX, 1996, Workshop in San Francisco, CA, USA, 30 Oct – 1 Nov. 1996, IEEE 30 October 1996, pp. 461-470) (the "Abnous reference") was cited in a supplemental EPO search report for the present invention. The Abnous reference discloses a heterogeneous array of satellite processors, some of which are also internally reconfigurable, while others are fixed (dedicated), with a switching communication network and a separate, global reconfiguration bus. The switching interconnect creates links between the satellite processors, as nodes, similarly to the arcs of a data flow graph. The Abnous reference also does not disclose and does not suggest the claimed features (1) – (7) above, such as the singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, the use of different mixes or combinations of computational elements to form different reconfigurable matrices, etc.

Eccles U.S. Patent No. 5,479,055 ("Eccles" or the "Eccles reference") and Wheeler et al. U.S. Patent No. 4,694,416 ("Wheeler" or the "Wheeler reference") were cited in the U.S. examination of a continuation-in-part of the cross-referenced, second related application, U.S. Patent Application Serial No. 10/384,486. Eccles discloses a switching matrix utilized to switch in or out different circuits having different functions.

Multiple instances of each different circuit are created, so that in the event of failure of one type of circuit, the failed circuit may be disconnected and another instance of the same circuit type may be connected, through the switching matrix. The Eccles reference also does not disclose and does not suggest the claimed features (1) – (7) discussed above.

The Wheeler reference discloses use of a plurality of identical operating units (multipliers/adders), with truncating and delay registers, coupled through multiplexers and demultiplexers to create configurable data paths. Configuration occurs through a separate and dedicated serial data bus, through serial connections between configuration registers. Identical units are cascaded to create different types of filters for signal processing. The Wheeler reference also does not disclose and does not suggest the claimed features (1) – (7) discussed above.

Two additional references were cited in the examination of the second related application, Marshall et al. U.S. Patent No. 6,353,841 ("Marshall" or the "Marshall reference") and Bertolet et al. U.S. Patent No. 5,910,733 ("Bertolet" or the "Bertolet reference"). Marshall merely discloses a repeating array of identical arithmetic logic units (ALUs) embedded in a switching fabric. These ALUs have the same inputs on every clock cycle. Marshall does not disclose the use of heterogeneous computational elements having fixed and differing architectures. The Marshall reference also does not disclose the claimed features (1) – (7) above. More particularly, the Marshall reference does not disclose or suggest a singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, etc. In addition, the Marshall reference does not disclose the use of different mixes or combinations of computational elements to form different reconfigurable matrices, and instead utilizes a repeating array of identical structures.

The Bertolet reference merely discloses known FPGA material which is provided in different sizes or amounts (based on row and column width of the repeating array), and is otherwise a repetitive array of identical computational units (core cells), with all remaining elements being traditional and repetitive FPGA interconnect. The

Bertolet reference also does not disclose and does not suggest the claimed features (1) – (7) above, such as the singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, the use of different mixes or combinations of computational elements to form different reconfigurable matrices, etc.

As a consequence, the cited references, alone or in combination, do not disclose and do not suggest all of the limitations of the independent claims of the present invention, such as the enumerated claimed features (1) – (7) above, of the independent claims 1, 32, 63, 89, 91, 93, and 94, as amended, and new independent claims 129 and 139 of the present invention. For example, the cited references do not disclose and do not suggest the singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, the multiple or nested levels of configuration, or the use of different mixes or combinations of computational elements to form different reconfigurable matrices, etc.,

In addition, in contrast to the interconnection network of the present invention used for both data and configuration, all of the references utilize separate data and configuration buses, thereby teaching away from the present invention. MPEP Section 2141.02. Such teaching away is the antithesis of art suggesting that a person of ordinary skill go in the claimed direction. See *In re Fine*, 873 F.2d 1071 (Fed. Cir. 1988). This teaching away from Applicants' invention is a *per se* and conclusive demonstration of lack of obviousness and a lack of anticipation.

Moreover, the patent office has not presented any motivation, suggestion or teaching to combine any of these references. Accordingly, no *prima facie* showing of potential obviousness has been made, and any assertions to the contrary have been clearly rebutted. In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Mills, 916 F.2d 680 (Fed. Cir. 1990). The rejection of claims 1 – 33 as anticipated under Section 102 and obvious under Section 103(a), therefore, should be withdrawn.

E. Other Cited Prior Art of Related Applications Also Does Not Disclose or Suggest the Claimed Features of the Invention.

The PCT Search Report of one of the PCT counterpart application, PCT/US02/37014, disclosed Harrison et al. U.S. Patent No. 5,963,048 and Wong et al. U.S. Patent No. 6,282,627, as not particularly relevant. The preliminary examination report found all 100 claims allowable over these references.

The PCT Search Report for the PCT application PCT/US2002/007101 disclosed Wasson U.S. Patent 6,433,578 ("Wasson" or the "Wasson reference") (and other references considered not to be particularly relevant). Wasson utilizes a first, non-reconfigurable array of identical, repeating units of "structured data path logic", having dedicated (non-reconfigurable) routing, each having fixed data I/O and dedicated data busses. Specifically, each bit-specific sub-block receives inputs (databus bits) from the immediately adjacent block, and the dedicated structured logic is not reconfigurable. Wasson Figures 12, 13 and 16, Col. 7, ll. 24 – 27, 54 – 55, and Wasson claim 1. A second, adjacent array of programmable, repeating units of identical unstructured control logic, similar to FPGA material (core cell, Figure 11), is also utilized to provide common control signals for the first array (Figures 8 and 10 and 11; Col. 6, ll. 17 – 22). A ring of programmable interconnect is also provided to the pads at the edge of the IC (Figures 15 and 16) for I/O (106) for programmable routing within the second, unstructured array, while the first, structured array utilizes dedicated, non-reconfigurable data bus routing directly to and from the I/O pads (Wasson Figure 16, 1204, and Col. 8, ll. 4-13). The reconfigurability of the architecture of the Wasson reference is, therefore, limited to the second, unstructured array having repeating units of identical, non-heterogeneous control logic.

As a consequence, Wasson also does not disclose or suggest all of the limitations of the independent claims of the present invention, including the claimed features (1) – (7) above, such as the singular interconnect network for transfer of both data and configuration, an interconnect network having both routing and switching elements, the use of routing elements (in addition to switching elements) for configuration, or the multiple or nested levels of configuration, the use of different mixes or combinations of computational elements to form different reconfigurable matrices, etc.

Instead, by utilizing a first, non-reconfigurable array of repeated and identical structured data path logic units, and a second, reconfigurable array of repeated and identical FPGA-like units, Wasson also teaches away from the present invention.

The US and PCT Search Reports of a third commonly assigned applications, U.S. Patent Application Serial No. 09/871,049, filed May 31, 2001 and issued September 9, 2003 as US Patent No. 6,618,434, and its corresponding PCT/US02/16044, Ito U.S. Patent No. US 6,408,039 B1 (the "Ito patent" or the "Ito reference"). For a rake receiver for communication systems, the Ito patent provides a plurality of combination searcher and finger circuits (Fig. 1), which can operate in either as searchers or multipath receivers (Col. 3, l. 46 – Col. 4, l. 8). As illustrated in Fig. 2 of the Ito patent, however, each of these functions is performed by separate, dedicated ASIC circuits, with the searcher mode utilizing despreader and signal strength calculator circuits, and with the finger mode utilizing the output of the despreader, along with different and separate dedicated ASIC circuits, namely, a delay lock loop, a phase calculator, a walsh despreader, and a phase equalizer (Col. 3, l. 51 – Col. 4, l. 19). The Ito patent uses these entirely different, dedicated circuits to perform either searching or path reception in all of the various embodiments disclosed. As a consequence, the Ito patent discloses using one set of dedicated ASIC circuits for searching, and another set of dedicated ASIC circuits for path reception, with each of these circuits repeatedly duplicated to form the multiple combination searcher/fingers. When one set of dedicated ASIC circuits is operational, the other set of dedicated ASIC circuits forming the combination searcher/finger is non-operational and quiescent.

The Ito patent merely discloses providing many additional, duplicative dedicated ASIC circuits for either searching or path reception, resulting in circuits which can be called to function as needed. Ito does not disclose or suggest all of the limitations of the independent claims of the present invention, such as the configuration and reconfiguration of a plurality of heterogeneous computational elements, each having different fixed architectures, for different functions. Ito also does not disclose or suggest using different mixes and layouts of these fixed and different computational elements to form differing reconfigurable matrices for different functional and operational modes. Ito

also does not disclose or suggest the multi-tiered or "nested" reconfigurability of these heterogeneous computational elements through a plurality of interconnection networks. As a consequence, the Ito patent does not disclose and does not suggest the claimed features of the present invention.

IV. Summary.

None of the cited references disclose or suggest the claimed elements of the present invention. More specifically, the various references, alone or in combination with each other, do not disclose and do not suggest any of the following claimed elements: (1) an interconnection network comprising both routing elements and switching elements; (2) using routing elements for configuration; (3) using an interconnection network for transfer of both data and configuration information; (4) using an interconnection network for data commingled with configuration information as a single bit stream or as a combined packet structure; (5) different mixes or combinations of different computational elements forming independently configurable groups; (6) "nested" or multiple levels of configuration; and (7) "self-routing" of data and configuration.

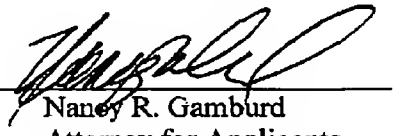
As a consequence, the cited references for this and related applications do not disclose and do not suggest the present invention. The present invention, therefore, is not anticipated and is not rendered obvious by these references under Sections 102 and 103, and the rejection of the claims should be withdrawn. In addition, because the remaining dependent claims incorporate by reference all of the limitations of the corresponding independent claims, all of the dependent claims are also allowable over the cited references.

On the basis of the above amendments and remarks, reconsideration and allowance of the application is believed to be warranted, and an early action toward that end is respectfully solicited. In addition, for any issues or concerns, the Examiner is invited to call the attorney for the applicant at the telephone number provided below.

Respectfully submitted,

Paul L. Master et al.

March 5, 2006

By 

Nancy R. Gamburd
Attorney for Applicants
Registration No. 38,147
Phone: 312-876-0460
Fax: 312-276-4176

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing second part of the Amendment And Response Under 37 CFR 1.111 And 1.115 (pages 1, 34-53 pages), and Transmittal (PTO/SB/21) (1 page), Transmission Receipts for original transmission on March 5, 2006 (2 pages), as 24 total pages, for Paul L. Master et al., Serial No. 09/997,530, entitled "Apparatus, System and Method For Configuration Of Adaptive Integrated Circuitry Having Fixed, Application Specific Computational Elements", originally faxed on March 5, 2006, have been re-transmitted by facsimile to the US Patent and Trademark Office to fax number (571) 273-8300 (Centralized Facsimile Number), on March 8, 2006.

Nancy R. Gamburd
Reg. No. 38,147